## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

KAWAGOE, et al.

Filed:

December 14, 2001

For:

PROCESS FOR MANUFACTURING A

SEMICONDUCTOR WAFER, A SEMICONDUCTOR

WAFER, PROCESS FOR MANUFACTURING A

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE,

AND SEMICONDUCTOR INTEGRATED CIRCUIT

**DEVICE** 

## INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 AND 1.98

Assistant Commissioner for Patents Washington, D.C. 20231

December 14, 2001

Sir:

Pursuant to Applicant's duty of disclosure, enclosed please find a List, on a form substantially equivalent to Form PTO-1449, of documents cited in connection with prior applications of the above-identified application, that is, application Serial No. 09/513,349, filed February 25, 2000, Serial No. 08/934,774, filed September 22, 1997 and Serial No. 08/508,483, filed July 28, 1995.

Since each of the documents on the enclosed List was cited in connection with at least one prior application of the above-identified application, that is, at least one of Serial No. 09/513,349, Serial No. 08/934,774 and Serial No.

08/508,483, being relied upon under 35 USC 120 in the present application, copies of the listed documents are not enclosed. See 37 CFR 1.98(d).

This Information Disclosure Statement is being submitted concurrently with the filing of the above-identified application. Accordingly, requirements of 37 CFR 1.97(b) are clearly satisfied.

In view of all of the foregoing, it is respectfully submitted that all applicable requirements of 37 CFR 1.97 and 1.98 have been satisfied, in connection with all documents on the enclosed List. Accordingly, consideration of the listed documents, upon examination of the above-identified application, is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.33873VC4) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

William I. Solomon

Registration No. 28,565

Tel.: 703-312-6600

WIS/slk Enclosures

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE	ATTY. DKT. NO.	SERIAL NO.	
	PATENT AND TRADEMARK OFFICE	501.33873VC4		
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U.S. PATENT DOCU	MENTS		20 d	

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA	4,835,740	5-89	Sato			
AB	5,290,714	3-94	Onozawa		1	
AC	4,761,384	8-88	Neppl			
AD	5,156,990	10-92	Mitchell			
AE	6,043,114	3-00	Kawagoe			
AF	4,564,416	1-86	Homma, et al.			
AG	4,684,971	8-87	Payne, et al.			
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AK	5,508,549	4-96	Watanabe, et al.			
AL	3,974,003	8-76	Zirinsky, et al.			

## FOREIGN PATENT DOCUMENTS

Examiner Documen Number	Document Number	Date	Country	Class	Subclass	Translation /Abstract	
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AM	0373723	6-20-90	Europe				
AN	0550021	7-85	Europe				
AO	60132358	7-85	Japan				
AP	58218159	12-83	Japan				
AQ	63157477	6-88	Japan				
AR	61002356	1-86	Japan				
AS							
AT						<u> </u>	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AU	Wolf, S., "Silicon Processing for the VLSI Era Vol. 1", ppg. 64-65.
AV	Ghandhi, S., "VLSI Fabrication Principles Silicon and Gallium Arsenide", ppg. 735-738.
AW	Yamaguchi, et al., "Process integration and device performance of a submicrometer BiCMOS with 16-GHz f(t) double Poly-Bipolar devices", IEEE Transactions on Electron Devices, Vol. 36, No. 5, ppg. 890-896.
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